WHAT IS CLAIMED IS:

1. A memory control circuit comprising a write error protect circuit that disables output of a write signal supplied from outside to a memory by resetting a register, outputs the write signal supplied from the outside to the memory upon writing a first data into the register, and prevents the output of the write signal to the memory upon writing a second data that is different from the first data into the register.

2. The memory control circuit according to claim 1, wherein the write error protect circuit includes

a first latch circuit that stores "0" by reset;

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input;

a first gate that outputs a register setting data supplied from the outside to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0"; and

a second gate that outputs a write signal supplied from the outside to the memory only when the output signal from the first latch circuit is "1".

3. A memory device comprising:

a memory that is rewritable by an input of a write signal from outside to the memory; and

a memory control circuit including a write error protect circuit

that disables output of the write signal by resetting a register, outputs the write signal to the memory upon writing a first data into the register, and prevents the output of the write signal to the memory upon writing a second data that is different from the first data into the register.

4. The memory device according to claim 3, wherein the write error protect circuit comprises:

a first latch circuit that stores "0" by reset;

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input;

a first gate that outputs a register setting data supplied from the outside to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0"; and

a second gate that outputs a write signal supplied from the outside to the memory only when the output signal from the first latch circuit is "1".

5. The memory device according to claim 3, wherein the memory is divided into a plurality of areas in which write disable, write enable, and write error protect are set independently; and the memory includes the write error protect circuit for each area.

6. The memory device according to claim 3, wherein the memory is a nonvolatile memory.

7. The memory device according to claim 6, wherein the nonvolatile memory is a flash memory.

8. A microcomputer comprising:

a central processing unit;

a memory that is rewritable by an input of a write signal from the central processing unit to the memory; and

a memory control circuit including a write error protect circuit that disables output of the write signal by resetting a register, outputs the write signal to the memory upon writing a first data into the register, and prevents the output of the write signal to the memory upon writing a second data that is different from the first data into the register.

9. The microcomputer according to claim 8, wherein the write error protect circuit comprises:

a first latch circuit that stores "0" by reset;

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input;

a first gate that outputs a register setting data supplied from the outside to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0"; and

a second gate that outputs a write signal supplied from the outside to the memory only when the output signal from the first latch

circuit is "1".

10. The microcomputer according to claim 8, wherein the memory is divided into a plurality of areas in which write disable, write enable, and write error protect are set independently; and the memory includes the write error protect circuit for each area.

11. The memory device according to claim 8, wherein the memory is a nonvolatile memory.

12. The memory device according to claim 11, wherein the nonvolatile memory is a flash memory.

13. The microcomputer according to claim 8, wherein the central processing unit, the memory, and the memory control circuit are integrated in a same semiconductor chip.